

## Electronics Status

*K. Einsweiler, LBNL*

### **FE-D and FE-H Status**

- FE-D submitted to TEMIC, expected back at CERN by end-October
- FE-H now getting organized

### **MCC Status**

- Completing MCC-D system design and developing real MCC testing tools

### **Power Supply and Opto-link Status**

- Power supply prototype status
- Optolink and optoelectronics status

### **Off-detector Electronics Status**

- Test System Status
- ROD and ROD Crate Status

## **FE-D Status**

### **FE-D Submission:**

- FE-D was submitted Aug. 10 after trying to resolve all remaining measurement, simulation, and verification issues.

### **Preparations for FE-D Testing:**

- Issues for operating with existing MCC: Several new features are not supported (new reset control, new error reporting, and self-trigger mode).
- Issues for operating with existing PLL: Need to support new features (new reset control, and self-trigger mode)
- Upgrades to PixelDAQ: Many small changes needed for register bits, and new features above. Complete PLL and PixelDAQ upgrades over next few weeks.

### **FE-D Status**

- Present status (as of yesterday) is that the fabrication is on schedule for wafers-out in mid-October, followed by 1 week for radiation testing, then delivery to CERN before the end of October.
- Expect TEMIC to ship eight wafers (guaranteed minimum). Each will have 106 potentially good die (with a fairly strict interpretation of the exclusion region). There are another 18 die that are worth at least testing for yield.

## Initial Testing Proposal

**Goal: test two wafers as quickly as possible and get them to Alenia and IZM for bump-bonding:**

- Do not dice any wafers before bumping, since there will only be eight in total.
- Carry out initial tests with PixelDAQ, supplemented to allow DAC characterization using a GPIB scanning ADC. If all goes well, may not need lower level testing.
- If there are any problems, we will have to resort to using the 200+ probe points Peter placed on FE-D, and verify where problems occur.
- **Two possibilities:** either John and I go to Bonn for a week in October and we do the testing in one place, or we do the work in parallel in Bonn and LBL. We prefer the latter, with frequent phone calls, etc. to deal with surprises and confusion.

**Can continue to use identical single-chip support cards:**

- Have 50 new cards at LBL, and also Bonn and Genova have design files and can (or have already ?) manufacture them independently.
- Once initial two wafers are bumped, some bare die and single-chip assemblies can be attached to these cards for lab and testbeam characterization.

**Other wafers to be tested and bumped after first lab results**

- First two FE-D wafers should keep us busy for a while.

- Assume that immediate module development needs can continue to be largely served by the remaining FE-B wafers (there are still a few more to go). We need to make another 4-6 modules at IZM soon (beyond two being delivered now).
- If all goes well, we may need to consider ordering supplemental FE-D wafers in early Spring in order to produce significant numbers of rad-hard modules and continue debugging the rest of the production sequence...

## Designing new **rad-hard single-chip card**:

- This card will use Laurent's buffer chip to replace all radsoft parts on present support card with single DMILL die.
- This card has the same geometry as the present single-chip card, and will allow us to irradiate single chip assemblies and operate them during irradiation.

## Should begin planning **near-term irradiation tests**:

- At LBL, plan to make use of 88" Cyclotron to irradiate single-chip assemblies as soon as possible (Nov or Dec ?) . How much work here before PS restarts ?
- In principle, we could do a complete module as well and just replace the non-critical chips on the module support card after irradiation. This would not allow operation during irradiation. Alternatively, we could produce a slightly modified Flex Support Card onto which Laurent's radhard buffer chip could be mounted.
- We should irradiate a Flex module with all passive components, MCC-DMILL test chip, and DMILL DORIC and VDC.

## FE-H Organization

### **Organization:**

- Have defined preliminary set of goals for the FE-H submission
- Most recent Honeywell update indicated that TAA agreements were progressing well, with expectation that within 3-4 weeks they should be in place.
- Have had first (short) designer discussion to organize near-term work. Franz is completing testing of prototype HSOI chip from 98. Gerrit is working on Cadence issues, and will then begin work on readout core of chip (column-pair). There are some final issues with the layout rules. Next steps (with TAA) will be for Giacomo to work on libraries, Laurent to work on front-end.

### **FE-H Manpower Update**

- Franz Pengg will be leaving at the beginning of November
- Gerrit Meddler is full time on this project, but will be based in Geneva until August 2000. He will carry the overall integration role.
- We presently have a new, and very capable young engineer in Berkeley, Emanuele Mandelli, who worked already on FE-D at the very end, and will work on FE-H.
- Laurent will work on the front-end design from CPPM

- Bonn will include Mario Ackers and Giacomo Comes again, but Mario will stop at some time and complete his thesis. Peter's role will be largely advising and supervising, as he has many other commitments to fulfill in Bonn.
- Overall, this is a very small and widely-distributed team, so there will be many challenges to complete the chip. We are looking for an additional person at LBL, but I do not expect anyone on this timescale.
- We will see how this effort progresses. If the initial schedule (submission in roughly Feb. 00) cannot be met by a significant amount, and FE-D works well, we will have to consider a fall-back where we adopt FE-D for the outer layers directly.

## **MCC Status**

- Prototype DMILL MCC (including FIFO and re-designed command decoder) was submitted to TEMIC with FE-D.
- Significant testing of AMS MCC has been carried out over last few months. Several minor problems have been identified, but the basic design works well.
- Giovanni has made a large effort to finalize remaining design issues for production MCC. A long design discussion this week has agreed on most open questions. Small iterations will occur over coming month, assisted by simulation.
- Serious design of the “pre-production” MCC can begin very shortly. The goal remains to submit this design to TEMIC in Feb. 00. This is very ambitious !
- We must also consider how to submit: multi-project runs do not give many large chips, and there would not be a strong motivation for another engineering run on this timescale. The best match I could imagine would be to submit a new reticle with 2 FE-D and a full MCC (DMILL reticle can be very large). However, this would give too many MCC and not enough FE-D...
- Progress is being made on the MCC test system in Genova, but it is very late. Most debugging of the present MCC has been done with PLL's (painful and incomplete). The addition of this complex and comprehensive tool is very important for our continued module development.

## **Power Supply Prototype Status**

### **First prototype path involves ISEG and Wiener:**

- HV supply received and evaluated by Wuppertal using real electronics. No particular problems observed, but interface is crude.
- Low voltage multi-channel “bulk-supply” can be requested from Wiener for evaluation. We will go ahead and do this soon.
- Problem with this solution is that it does not address integration and control issues which are vital for our final system.

### **Second prototype path involves CAEN:**

- After considerable discussion, a realistic prototype has been requested. The specifications are our present best-guess for a “multiplicity two” supply.
- There are seven supplies in each complex channel. Each supply is floating, and there is internal voltage-drop compensation. There is a programmable power-on sequence and one interlock input.
- Order was delayed due to funding delays in Italy, but is now in the process of being placed. Delivery should be early Spring.
- Significant concerns about cost of this path, and risk associated with single vendor, but it is presently the only system which addresses our complete needs.

## Optolink Status

### **Opto-electronics:**

- As part of the TEMIC FE-D submission, there were two opto-electronics chips submitted as well. These were designed by OSU and Siegen.
- These are modified “all-CMOS” versions of the SCT VDC and DORIC, referred to as VDC-P and DORIC-P. The designs have been simplified to meet our needs. They can be integrated into MCC, or remain separate die on an opto-hybrid, depending on the opto-link placement. Initial testing will be done at Siegen and Wuppertal, followed by integration with opto-packages and modules.

### **Opto-components:**

- Further studies of VCSELs with proton irradiation at PS. First results look encouraging, but there are some issues with dose normalization in the GaAs VCSEL.
- Measurements of a complete link in ISIS at pixel fluences have also been made. The results indicated the presence of noticeable SEU, which was traced to energy depositions in the epitaxial PIN diode. This can be partially compensated by an increase in ROD drive power for the TTC fiber. However, as an additional measure, we have proposed to adopt a much more robust protocol for TTC for the final MCC (5-bit fast messages with single-bit error correction instead of the original 3-bit messages). This should allow the operation of our modules in the presence of significant SEU induced errors.

## Test System Status

**Have begun design of a more complete and powerful test system for FE wafer probing and possibly production module testing.**

**This would permit several forms of more rigorous testing to be done:**

- Parametric testing of chips and modules with parameters being increased XCK frequency, as well as variations of amplitudes and timing of each input and output signal. This will allow real evaluation of how far each chip and module exceeds our basic specifications. In this way, we can place cuts to guarantee that chips and modules should continue to work after irradiation with some given confidence level.
- More programmability to allow adapting of the test system to presently unknown new needs
- More memory to allow complete module level scans to be performed on-board. This should allow a factor 3 improvement in module scan speed, allowing a complete threshold scan in about 20 minutes for a 50K channel module.
- Anticipate that this system should be ready to operate by about March 00, contingent on finding some additional manpower at LBL.

## **ROD Status**

- Quite functional, combined SCT/Pixel off-detector electronics effort is now coming into being.
- Two day workshop at UCL in July attended by Giovanni and myself. Monthly meetings among ROD effort head, and SCT+pixel electronics coordinators at LBL. Significant review of prototype design anticipated in Oct./Nov. timeframe.
- ROD architecture is fairly complete and much VHDL coding is already complete. Simulations are continuing to define link multiplicity and number of modules per ROD module.
- On track to deliver first prototypes for user evaluation for user community to evaluate by about May 00.

## **System Test:**

- The schedule above fits well with the need for pixels to organize at least one system test in a June/July timeframe. This should include many modules (at least 3-4), mounted on realistic cooling structures with plausible clearances, and read out by optolinks.
- This would be a first chance to experience multi-module problems first-hand.
  - Ideally this would occur in more than one place, but as a minimum this will be a major goal at LBL next Summer. A second site (Bonn ?) working on staves would seem a desirable goal.